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10/750,075	12/31/2003	Louis Lippincott	ITL.1703US (P17498)	2083

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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,075	LIPPINCOTT ET AL.	
	Examiner	Art Unit	
	Chikaodili E. Anyikire	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *4 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 September 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed September 13, 2007 have been fully considered but they are not persuasive. Claims 1-22 are currently pending.

2. The applicant amended claim 1 to state the following language, "most significant", which does not put it in condition for allowance. The reference, Lin (US 6,421,466), reads, "Width reduction can be performed by taking the most significant bits (MSBs)", and therefore reads on the applicant's claim 1 (Col 8 Ln 15-23). For claim 18, argument analogous to those presented for claim 1 are applicable for claim 18. Claim 8 also argues about the most significant bits, which the applicant is referred to the arguments for claim 1. Claim 13, the applicant introduces a circuit to mask the most significant bits. The applicant is referred to Fig 4, element 62 (width reducer) and Col 8 Ln 15-23, which disclose the circuit and the ability to take the most significant bits.

A detailed rejection addressing the newly added limitations follows.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US 6,421,466).

As per claim 1, Lin discloses a method, comprising:

a) taking the absolute difference of:

1) less than all of the bits of an uncompressed video data value from a reference macro block (Fig 4, 52);

2) less than all of the bits of an uncompressed video data value from a macro block worth of data within a search window (Fig 4, 42; Col 5 Ln 45-50);

b) calculating a sum of absolute differences between corresponding data values within said reference macro block (Fig 4, 52) and said macro block worth of data (Fig 4, 42), said absolute difference being one of said absolute differences (Col 6 Ln 60 – Col 7 Ln 7); and

c) calculating a motion vector based upon the position of said reference macro block (Fig 4, 52) in a first frame and the position of said macro block worth of data (Fig 4, 42) in said second frame, said sum of absolute differences being a lowest sum of absolute amongst other sums of absolute differences calculated between said reference macro block (Fig 4, 52) and other macro blocks worth of data (Fig 4, 42) within said search window (Col 7 Ln 1-17).

As per claim 2, Lin discloses the method of claim 1 wherein said first frame is a current frame (Fig 4, current pic) and said second frame is previous frame (Fig 4, Old pic; Col 5 Ln 45-50).

As per claim 3, Lin discloses the method of claim 1 further comprising loading said reference macro block's data values (Fig 4, 52) into a register (Fig 5, 92) prior to said taking (Col 7 Ln 19-31).

As per claim 4, as best understood by the Examiner, Lin discloses the method of claim 1 wherein said reference marcoblock's data values (Fig 4, 52) are uncompressed when said loaded reference macroblock (Col 5 Ln 45-50; prior art discloses full resolution picture, which refers to an uncompressed image).

As per claim 5, Lin discloses the method of claim 3 further comprising loading said search window's data values (Fig 4, 42) into a random access memory prior to said taking the absolute difference (Col 7 Ln 19-31).

As per claim 6, as best understood by the examiner, Lin discloses the method of claim 5 wherein said reference marcoblock's data values (Fig 4, 52) are uncompressed when said loaded and said search window's data values are uncompressed when loaded (Fig 6, Col 7 Ln 40-51).

As per claim 7, as best understood by the examiner, Lin discloses the method of claim 1 further comprising determining which N bits from:

1) said reference macroblock's data value's M bits (Fig 4, 52; Col 8 Ln 15-23; data value has been considered to be an 8-bit pixel value)

2) said search window macro block's data value's M bits (Fig 4, 42) are to be used for said taking the absolute difference (Col 8 Ln 15-23; the prior art discloses M=8 bits having been reduced to N=6 bits for the absolute difference calculation).

As per claim 13, Lin discloses an apparatus, comprising:

a) logic circuitry to take an absolute difference between:

1) less than all of the bits of an uncompressed video data value from a reference macro block (Fig 4, 52);

2) less than all of the bits of an uncompressed video data value from a macro block worth of data within a search window (Fig 4, 42; Col 5, Ln 35-50);

b) a register (Fig 5, 92) to store said reference macro block (Fig 4, 52), said register coupled to said logic circuitry (Fig 7, Ln 19-31); and

c) a random access memory to store said search window said random access memory (Fig 5, 92) coupled to said logic circuitry (Col 7 Ln 19-31).

As per claim 14, Lin discloses the apparatus of claim 13, further comprising adding an offset value to said reference macro block's uncompressed video data value and said search window macro block's uncompressed video data value (Col 3 Ln 51-Col 4 Ln 14; generating images with reduced_width level pixel data will add an offset to the pixel values and change the optical resolution of the reference and search window macroblocks).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 8, 9, 11, 12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,421,466) in view of Pourreza et al ("Weighed Multiple Bit-Plane Matching, A Simple and Efficient Matching Criterion for Electronic Digital Image Stabilizer Application).

As per claims 8 and 17, Lin discloses the method of claims 8 and 17, wherein said determining comprises:

determining the number of most significant bits that are to be masked from both said data values (Col 8 Ln 15-18);

Lin does not disclose determining the number of least significant bits that are to be masked from both said data values.

In the same field of endeavor, Pourreza et al teaches reducing the complexity of block matching criterion by truncating different combination of the bits of 8-bit pixels that includes masking a number of most significant bits or less significant bits accomplished on SSD, SAD, MPDC, BPROP, sub-sampled BPROP or BPROPS (4 to 1 sub-sampling), Ko method (by using $b_1b_2b_3b_4$, $b_2b_3b_4b_5$, $b_3b_4b_5b_6$ and $b_4b_5b_6b_7$ bits) matching criteria(Fig 3 Section 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the method of Lin with the method of Pourreza et al. The advantage of the integration is that it will reduce the complexity of block matching process and has the best performance than other 1 bit-per-pixel algorithms (Pourreza, Section 5).

As per claim 9, as best understood by the Examiner, Lin discloses the method of claim 8 wherein said determining the number of least significant bits is (N-M)-(said determined number of most significant bits) (Col 8 Ln 15-23; the prior art teaches selecting 6 bits as the most significant bits, which represents using N=6 bits from 8-bit pixels, and therefore the leftover bits will represent the least significant bits).

As per claim 11, Lin disclose the method and apparatus of claims 9, further comprising adding an offset value to said reference macro block's uncompressed video data value and said search window macro block's uncompressed video data value (Col

3 Ln 51-65, generating images with reduced_width level pixel data will add an offset to the pixel values and change the optical resolution of the reference and search window macroblocks).

As per claims 12, Lin discloses the method of claim 11 wherein said offset is set equal to a minimum valued uncompressed video data value of said reference macro block (Col 3 Ln 51- Col 4 Ln 14; the prior art discloses reducing pixel values to a reduced_width level 4 image, which is the minimum and is used as an offset).

6. Claims 15, 16, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,421,466) in further view of Kondo et al (US 2004/0120197).

As per claims 15 and 20, Lin discloses circuitry for adding offset values (generating level_1 through level_4 reduced_width image pixels) to reference macroblock's uncompressed video data values (Col 3 Ln 51- Col 4 Ln 14; Fig 5, DSP 90).

Lin does not explicitly disclose the first adder and detail of logical circuitry.

In the same field of endeavor, Kondo et al disclose well-known circuitry for implementing SAD (Sum of Absolute Differences) as part of motion compensation (MC) prediction coding device that includes adders (Fig 9-12, 20 and 21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify Lin's invention to explicitly illustrate

different components of logic circuitry because it will provide detailed information concerning well known logic circuitry for SAD and MC.

Regarding claims 16, 20, and 21, arguments analogous to those presented for the rejection of claim 15 are applicable to claims 16, 20, and 21. Inputs to circuitry shown on Figs 9-12 are reference macroblock's and search macroblock's video data.

As per claim 18, Lin discloses an apparatus, comprising:

a) logic circuitry to take an absolute difference between:

1) less than all of the bits of an uncompressed video data value from a reference macro block (Fig 4, 52);

2) less than all of the bits of an uncompressed video data value from a macro block worth of data within a search window (Fig 4, 42; Col 5, Ln 35-50);

b) a register (Fig 5, 92) to store said reference macro block (Fig 4, 52), said register coupled to said logic circuitry (Fig 7, Ln 19-31); and

c) a random access memory to store said search window said random access memory (Fig 5, 92) coupled to said logic circuitry (Col 7 Ln 19-31).

However Lin does not explicitly teach d) a DRAM memory coupled to said register and said random access memory, said DRAM memory to store said uncompressed video data value from a reference macro block and said uncompressed video data value from a macroblock worth of data within a search window.

In the same field of endeavor, Kondo et al teach FIG. 14 shows a configuration of an exemplary DRAM cell. Capacitors C1 and C2 are connected in series, and a voltage Vcc/2 (Vcc being a power supply voltage) is supplied to the midpoint P of capacitors C1 and C2. One end of capacitor C1 opposite the point P is defined to be the memory node N1, which node is connected with a bit line BL via access transistor Q7 having its gate connected to the word line WL ([0144]).

It should be understood that if memory cell 140 is DRAM-cell based one, its memory cell unit 141 is configured like memory cell unit 13 of the SRAM cell shown in FIG. 13, and if memory cell 140 is DRAM-cell based one, its memory cell unit 141 is configured like memory cell unit 14 of the DRAM cell shown in FIG. 14 ([0149]).

It is noted here that n ancillary operational cells 150 corresponding to given pixel data (n bits) of the candidate block obtain subtraction value output given by subtracting the pixel data of the associated reference block from the pixel data of the candidate block. That is, denoting by Xi and Yi (i=0, 1, . . . , n-1) the given pixel data of the candidate block and the pixel data of the corresponding reference block, respectively, the operation output Si and the carry output Ci are obtained according to the following formulas (1) and (2), respectively, by supplying /Yi (/Yi expressing Yi overscored, representing inverted data Yi) as reference data RD of the memory cell 140 described above, and by setting C.sub.-1=1:

Si=Xi.sym.[overscore (Yi.sym.)]Ci-1 (1) ([0171]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the method of Lin with the DRAM of Kondo et al. The advantage of using DRAM is that it provides a high transfer rate and temporarily accumulated in a register to form a necessary tap or necessary pixel block.

As per claim 19, Lin discloses the apparatus of claim 18 further comprising adding an offset value to said reference macro block's uncompressed video data value and said search window macro block's uncompressed video data value (Col 3 Ln 51-Col 4 Ln 14; generating images with reduced_width level pixel data will add an offset value to the pixel values and change the optical resolution of the reference and search window macroblocks).

7. Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,421,466) in further view of Kondo et al (US 2004/0120197), as applied to claim 18 above, and further in view of Pourreza et al ("Weighed Multiple Bit-Plane Matching, A Simple and Efficient Matching Criterion for Electronic Digital Image Stabilizer Application).

As per claim 22 Lin discloses the method of claim 18, wherein said determining comprises:

determining the number of most significant bits that are to be masked from both said data values (Col 8 Ln 15-18);

Lin does not disclose determining the number of least significant bits that are to be masked from both said data values (Col 8 Ln 15-23; the prior art discloses that other methods can be used such as choosing the least significant bits (LSBs)).

In the same field of endeavor, Pourreza et al teaches reducing the complexity of block matching criterion by truncating different combination of the bits of 8-bit pixels that include masking a number of most significant bits or less significant bits, accomplished on SSD, SAD, MPDC, BPROP, sub-sampled BPROP or BPROPS (4 to 1 sub-sampling), Ko method (by using $b_1b_2b_3b_4$, $b_2b_3b_4b_5$, $b_3b_4b_5b_6$ and $b_4b_5b_6b_7$ bits) matching criteria(Fig 3, Section 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to integrate the method of Lin as modified by Kondo et al with the method of Pourreza et al. The advantage of the integration is that it will reduce the complexity of block matching process and has the best performance than other 1-bit-per-pixel algorithms (Pourreza, Section 5).

Allowable Subject Matter

8. Claim 10 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chikaodili E. Anyikire whose telephone number is (571) 270-1445. The examiner can normally be reached on Monday to Friday, 7:30 am to 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272 - 7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CEA